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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,546	03/30/2001	Jin-Yuan Lee	MEG2000-012	4705

28112 7590 10/06/2006

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EXAMINER

OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/821,546	LEE ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Douglas W. Owens	2811	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) See Continuation Sheet is/are allowed.
- 6) ☒ Claim(s) 63, 65, 66, 68, 71, 127-129, 132, 133, 165-168 and 181-184 is/are rejected.
- 7) ☒ Claim(s) 64, 67, 69-74, 131 and 162-164 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____  | 6) <input type="checkbox"/> Other: _____                                    |

Continuation of Disposition of Claims: Claims pending in the application are 11-13,15,17,19,20,23-25,42-58,60-71,73,74,102-107,109-111,117-121,123-129,131-141 and 143-188.

Continuation of Disposition of Claims: Claims allowed are 11-13,15,17,19,20,23-25,42-58,60-62,102-107,109-111,117-121,123-126,134-141,143-161,169-180 and 185-188.

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September, 18, 2006 has been entered.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 63, 65, 66, 68, 71, 127 – 129, 132, 133, 165 – 168 and 181 – 184 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,165,885 to Gaynes et al.

Regarding claim 63, Gaynes et al. teach a method of forming an electronic package (Fig. 1) comprising the steps of:

joining at least a substrate with die therein and a substrate (114), wherein an opening (116) is formed in the substrate and exposes a topmost patterned circuit layer of said die; and

depositing a conductive material into the opening (118), wherein the conductive material is suited for connecting said topmost patterned circuit layer to an external circuitry. With respect to using the conductive material to connect to external circuitry, this is considered a suggested use limitation and is not given any patentable weight. (See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967); *In re Otto*, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963)).

With respect to the limitation of joining the substrate with the die, it has been held that the selection of any order of process steps is *prima facie* obvious in the absence of new or unexpected results. See *Ex parte Rubin*, 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render *prima facie* obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Additionally, Gaynes et al. teach that the step of dicing may be performed at any point in the process (Col. 17, lines 46 – 50).

Regarding claim 65, Gaynes et al. teach a method, wherein the conductive material comprises tin-lead alloy or tin-silver alloy (Col. 15, lines 45 – 51).

Regarding claim 66, Gaynes et al. teach a method, wherein the external circuitry comprises a next level of packaging.

Regarding claim 68, Gaynes et al. teach a method, wherein the die comprises multiple pads (104) exposed by the openings in the substrate and exposed by multiple openings in a passivation layer (108) formed over an active surface of the die.

Regarding claims 71 and 129, Gaynes et al. teach a method, after joining the die to the substrate, further comprising forming a polymer layer encapsulating the die (Col. 19, lines 14 – 25).

Regarding claim 127, Gaynes et al. teach a method of forming an electronic package comprising the steps of:

providing a die comprising a pad (104) and a passivation layer (106), an opening in the passivation layer (108) exposing the pad; and

joining the die and a substrate, an opening in the substrate exposing the pad (114, 116).

Regarding claim 128, with respect to forming the opening before joining the die and substrate, It has been held that the selection of any order of process steps is prima facie obvious in the absence of new or unexpected results. See *Ex parte Rubin*, 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Regarding claim 132, Gaynes et al. teach a method, after joining said die to the substrate, further comprising depositing a conductive material into the openings (118).

Regarding claim 133, Gaynes et al. teach a method, wherein the conductive material comprises multiple solder balls (1509).

Regarding claims 165 and 127, Gaynes et al. do not teach a method, wherein the thickness of the substrate is between 150 and 300 microns. The thickness of substrates is a known result effective variable that is subject to optimization. It would have been obvious to one of ordinary skill in the art to find the optimal thickness of the substrate through routine experimentation (*In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977)).

Regarding claims 166, 167, 182 and 183, Gaynes et al. teach a method wherein the opening is formed by laser or mechanical drilling (Col. 13, lines 19 – 22).

Regarding claims 168 and 184, Gaynes et al. do not teach a method, wherein the substrate comprises BT. BT is a known material that is commonly used in the semiconductor art. It would have been obvious to one of ordinary skill in the art to use BT for the substrate, since it is a known material that is well suited for the intended use. The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

#### ***Allowable Subject Matter***

4. Claims 64, 67, 69, 70, 73, 74, 131, 162, 163, 164 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

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independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 11 – 13, 15, 17, 19, 20, 23 – 25, 42 – 58, 60 – 62, 102 – 107, 109 – 111, 117 – 121, 123 – 126, 134 – 141, 143 – 161, 169 – 180 and 185 – 188 are allowed.

### ***Response to Arguments***

6. Applicant's arguments filed September 18, 2006 have been fully considered but they are not persuasive.

Applicant argues that Gaynes et al. fail to teach, hint or suggest the step of joining a die, but not a wafer, to a substrate. Gaynes teach that the step of singulating the wafer may be performed at any point in the process (Col. 17, lines 46 – 50). Applicant asserts that Gaynes et al. do not teach the “detailed steps” if the substrate is not diced at the end of the process. One having ordinary skill in the art would have a clear understanding of how to join the die after singulation from the wafer. Furthermore, the Applicant has not presented evidence in support of the allegation that this teaching by Gaynes et al. is not enabled as far as one having ordinary skill in the art would be concerned.

Applicant further traverse's the opinion that “the order of process steps is prima facie obvious in the absence of new or unexpected results.” Applicant has further asserted that this is the opinion of the Examiner. This is not the sole opinion of the Examiner, but established case law. Applicant has failed to present evidence that dicing the wafer before attaching it to the substrate would have resulted in any new or unexpected results.

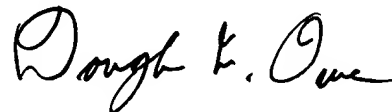


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Douglas W Owens  
Primary Examiner  
Art Unit 2811